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Patent Application for:

BUS FILTER FOR MEMORY ADDRESS TRANSLATION

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BUS FILTER FOR MEMORY ADDRESS TRANSLATION

FIELD OF THE INVENTION

This invention relates generally to the field of micro-controller memory management. More particularly, this invention relates to a bus filter for translating from virtual memory addresses to physical memory addresses.

BACKGROUND OF THE INVENTION

Digital systems often comprise a number of functional blocks connected by one or more bus structures. An example of a functional block is special purpose accelerator, such as a vector processor or image processor. Functional blocks may be connected using a number of different bus architectures, such as AMBA (Advanced Micro-controller Bus Architecture). AMBA is an open standard, on-chip bus specification that details a strategy for the interconnection and management of functional blocks that make up a System on-Chip (SoC). Special purpose accelerator blocks outside of a processor core often do not have access to the memory address translation functions provided by the processor code, or along the datapath between the code and the main bus. Such devices are usually restricted to "physical addresses" (addresses in a physical memory space), forcing programming model changes to make them useful.

When a system is initialized, large "worst case" contiguous memory regions must be allocated for use by these accelerators. This prevents memory from being allocated at run-time and does not allow non-contiguous memory to be used.

Sun Workstations, circa 1990, used a feature called "DVMA" which allocated some virtual space for device use. However, this feature worked with a restricted address range and its primary intent was to reduce the need for cache flushing in a virtual cache environment.

Special purpose accelerators are used in many applications, including cellular telephones, digital cameras, PDAs and automotive collision avoidance devices.

SUMMARY OF THE INVENTION

The present invention relates generally to micro-controller memory management. Objects and features of the invention will become apparent to those of ordinary skill in the art upon consideration of the following detailed description of the invention.

In one embodiment of the invention, a bus filter translates between virtual and physical memory addresses. The bus filter may be used to couple a processing device, such as an accelerator, to a system having a core processor and an external memory unit coupled by a bus. The bus filter includes a first bus interface connected to the bus for receiving a virtual memory address and a second interface connected to the bus for transmitting a physical memory address. An address translation unit, such as a translation lookaside buffer, determines the physical memory address from the virtual memory address.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as the preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawing(s), wherein:

FIG. 1 is a diagrammatic representation of an exemplary system incorporating a bus structure.

FIG. 2 is a diagrammatic representation of an exemplary system incorporating a bus structure and an address translation filter of the present invention.

FIG. 3 is flowchart depicting a method of operation of an address translation filter in accordance with an embodiment of the present invention.

FIG. 4 is a diagrammatic representation of an address translation filter in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail one or more specific embodiments, with the understanding that the present disclosure is to be considered as exemplary of the principles of the invention and not intended to limit the invention to the specific embodiments shown and described. In the description below, like reference numerals are used to describe the same, similar or corresponding parts in the several Views of the drawings.

Devices, such as special purpose accelerators, are usually restricted to "physical addresses" (addresses in a physical memory space), forcing programming model changes to make them useful. If such devices operated on "virtual addresses", most of these programming model difficulties would be removed. Such an option would also remove the need to allocate, at initialization time, large "worst case" contiguous memory regions for use by these accelerators. In turn, this would allow systems to be designed with smaller memory footprints.

An exemplary prior art system using a bus structure is shown in **FIG. 1**. Referring to **FIG. 1**, a core processor 100 includes a central processing unit (CPU) 102 that interfaces with an internal memory unit 104. In order to permit accesses to external memory, an address translator 106 couples the CPU via a bus structure 108 to an external memory unit 110. The address translator receives virtual (logical) addresses from the CPU and translates them into physical addresses for addressing the external memory 110. The translation may be performed using a virtual-to-physical memory map 112. This map may take the form of a lookup table. Using this system, the CPU can use virtual memory addresses. However, additional devices 114 and 116 that are coupled to the bus structure address the external memory directly and so must use physical addresses. This complicates the programming of the devices.

An exemplary system incorporating the present invention is shown in **FIG. 2**. Referring to **FIG. 2**, an address translation filter 118 of the invention is placed on the bus structure between one of the devices 114 and the external memory 110. The address translation filter has first and second interfaces to allow to be used a filter on a bus structure. The address translation filter passes memory addresses from the

attached device 114 through a TLB (translation lookaside buffer), allowing a virtual-to-physical address translation instead of using only physical addresses. This simplifies the programming of the attached device 114. Generally, the buses on either side of the address translation filter are of the same type. Since the buses operate under the same protocol, no protocol translation is required. The address translation filter performs virtual-to-physical address translation. The virtual memory may have a different width to the physical memory.

When the attached device is programmable, code may be transferred from the core processor to the attached device via the bus. The memory map in the address translation filter may be initialized at the same time, thereby reducing the time spent refreshing the map during operation of the code.

The invention may be used with a variety of different bus architectures, but the AMBA will be used as an example. The address translation filter can be inserted between any device that interfaces to an AMBA bus and the AMBA bus. The AMBA bus protocols are robust enough to handle any extra cycles of delay introduced by the filtering device. Such extra cycles appear to the attached device as a slightly slower memory system.

An exemplary embodiment of the method of operation of an address translation filter of the present invention is shown in the flowchart of **FIG. 3**. Following start block 300 in **FIG. 3**, the filter receives in input bus signal at block 302. In general, not all bus signals contain memory addresses, so at decision block 304 a check is made to determine if the bus signal contains a memory address. In one embodiment, the address is tagged as virtual address or a physical address. In a

further embodiment, all addresses are assumed to be virtual addresses. If the bus signal does not specify a virtual address, flow returns to block 302 as depicted by the negative branch from decision block 304.

If the bus signal specifies a virtual address, as depicted by the positive branch from decision block 304, a check is performed at decision block 306 to determine if the address is contained within an address translation unit in the filter. The translation unit may take the form of a translation lookaside buffer (TLB) indexed by the virtual address (or the most significant portion of the address). If no entry exists on the table for the address, as depicted by the negative branch from decision block 306, the device making the request is paused or stalled at block 308. The lack of a matching address in the table is referred to as a TLB miss. TLB misses appear to the device as very slow memory, this apparent time being the time that it takes for some TLB reload mechanism to determine and load the correct mapping. Again, the bus protocols provide for variable memory speeds and the attached device must already handle this case. In power-sensitive environments, the clock signal may be routed through the address translation filter to the device, so that during the time when a TLB miss (missing translation) has occurred, the clock to the attached device can be suppressed. This may reduce the total power consumption in the device by eliminating any power use during such times when it is known to be stalled. If no entry exists in the table, the table is refreshed at block 310. Since the address translation filter itself appears on the AMBA bus, the processor core and system software can manage the TLB mappings, including when there is a "TLB miss", because the device requested an address that has not yet been loaded into the filter. In

one embodiment of the invention, the filter sends a control signal, or interrupt, to the core processor and the processor responds by replacing an entry in the table by an entry corresponding to the unmatched address. The least used entry or the entry not used for the longest time may be replaced. To facilitate this, the filter may keep track of table accesses.

At block 312 the physical address corresponding to the virtual address is retrieved from the table. At block 314 the physical address is passed to the bus structure to facilitate the appropriate memory access. Flow then returns to block 302.

FIG. 4 is a diagrammatic representation of an address translation filter 118 in accordance with an embodiment of the present invention. Referring to **FIG. 4**, the filter 118 has a first interface to receive a bus signal 400 from a device. The address portion of the signal typically comprises P bits specifying a page number 402 and D bits specifying an offset 404 from the start of the page. A TLB (translation lookaside buffer) or other address translation unit 406 provides a map linking the pages of virtual memory to frames of physical memory. The physical memory is typically smaller than the virtual memory. The memory frame is specified by F bits. The physical address comprises the frame address 408 and the offset 410. In practice, the bits specifying the offset may be simply passed through the address translation filter. The physical address is transmitted via a second interface to the bus structure at the output of the filter 412.

Referring still to **FIG. 4**, the address translation filter includes refresh logic 414. If a TLB miss occurs, the logic informs the core processor via link 416. This link may be a control line separate from the bus structure (such a hardware interrupt

line) or the information may passed via a control vector on the bus structure itself. In one embodiment, the core processor determines how the TLB should be updated, using the bus structure to interrogate the address translation filter and to send new table entries to refresh the TLB. A system clock signal 418 may be received by the refresh logic and selectively passed to the attached device via link 420. If a TLB miss occurs, the device clock is paused until the TLB is refreshed. This mechanism may reduce the power consumption of the attached device.

The device of the present invention resolves several problems related to virtual and physical mapping. By providing virtual to physical mapping in the TLB, the programmer need not do such translation as part of setting up the attached device; the system software can use the translation tables for the host program for the information needed in the address translation filter. It also alleviates the requirement that such attached devices need contiguous memory regions for their work. Where such attached devices formerly required the allocation of these contiguous blocks at system initialization time, before memory becomes fragmented, the invention allows the allocation to be deferred until the device is actually used; this results in a net reduction in total memory required for such a system.

Those of ordinary skill in the art will recognize that the present invention could be implemented using a variety of hardware components, such as special purpose hardware, general purpose computers, microprocessor based computers, digital signal processors, microcontrollers, dedicated processors, custom circuits, ASICS and/or dedicated hard-wired logic.

The address translation filter of the invention may be configured to interface with a variety of bus structures, including the AMBA bus mentioned above and the AHB (Advanced High-performance Bus).

While the invention has been described in conjunction with specific embodiments, it is evident that many alternatives, modifications, permutations and variations will become apparent to those of ordinary skill in the art in light of the foregoing description. Accordingly, it is intended that the present invention embrace all such alternatives, modifications and variations as fall within the scope of the appended claims.

What is claimed is: